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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,861	01/05/2001	Lewis A. Morrow	YOR9-2000-0472US1 (8728-4	3687

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Frank Chau, Esq.
F. Chau & Associates, LLP
Suite 501
1900 Hempstead Turnpink
East Meadow, NY 11554

EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2185	3

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,861	MORROW ET AL.	
	Examiner	Art Unit	
	Paul B Yanchus	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Cai, US Patent no. 6,501,999.

Regarding claims 1 and 10, Cai teaches a computer system comprising:

at least two processing units having different energy efficiencies and adapted to at least execute tasks based on processing requirements of the tasks and a corresponding processing capablility [column 2, lines 46-67]; and

a scheduler [processor arbitration mechanism] adapted to schedule a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to reschedule the given task for execution by another of said at least two processing units when a determination indicates that one of said at least two processing units is unable to accommodate execution of the given task based upon the processing requirements of the given task and the corresponding processing capability [column 3, lines 25-48].

Cai teaches a scheduler [processor arbitration mechanism], which attempts to execute tasks on the power efficient processor, during battery operation mode, until it is determined that

the high-performance is needed to execute a particular task, such as processing graphic data. The high-performance processor is then powered up execute the task [column 3, lines 25-48].

Regarding claim 2, it is inherent in the teachings of Cai that the task execution end time is considered when analyzing the processing requirements for the task. Cai teaches that tasks concerning processing graphic data require a high-performance processor for execution. It is essential that graphical data be processed by a certain time so it can be displayed to a user without a noticeable delay.

Regarding claims 3 and 4, Cai teaches that the processor arbitration logic is part of host interface circuitry. Cai teaches that the host interface logic may be on the same die as the power efficient processor. Therefore Cai suggests that the processor arbitration logic may be embodied within the same hardware component as one of the processors or within a separate hardware component [column 4, lines 27-35 and Figure 1].

Regarding claims 5-7, Cai teaches that the two processors share system memory and I/O space and use the host interface to access the shared memory, I/O space and PCI bus [column 4, lines 5-35 and Figure 1].

Regarding claim 8, Cai teaches that the two processors and the host interface share system memory and I/O space [column 4, lines 5-35 and Figure 1].

Regarding claim 9, it is inherent that some type of task attribute store would have to be used by the processor arbitration logic in order to successfully identify which tasks require high-performance processing and which tasks can be executed on the power efficient processor.

Regarding claim 13, Cai teaches that the processor arbitration mechanism selects the proper processor based on predetermined criteria, such as processing power [column3, lines 35-45].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 and 14-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cai, US Patent no. 6,501,999, in view of Inoue, US Patent no. 4,954,945.

Regarding claims 11 and 12, Cai does not explicitly teach that the processors are able to determine whether they meet the processing requirements for executing a task and accepting or rejecting the task accordingly. Inoue teaches a multi-processor system, in which each processor determines whether it can execute a task and outputs a corresponding accept or reject signal [column 3, lines 22-45].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Cai and Inoue. Enabling each processor to determine whether or not it can successfully execute a process according to certain requirements would allow for less complex task scheduling circuitry since the task scheduling circuitry would no longer need to determine processor capabilities.

Regarding claims 14-21 and 23-30, Cai and Inoue teach a multiprocessor computer system, as described above. Cai also teaches attempting to execute a task on the most power efficient processor first. In battery operation mode, the power efficient processor is used to execute tasks until it is determined that a high-performance processor is needed to execute more processor intensive tasks.

Regarding claim 22, Cai and Inoue teach a multiprocessor computer system, as described above. It would have been obvious to one of ordinary skill in the art to exclude a processor from the partial order according to a predetermined condition, such as if there is not enough power in the system to power that processor.

Regarding claims 31-33, Cai and Inoue teach a multiprocessor computer system, as described above. Also, Inoue teaches that each processor stores a task table containing the tasks that the processor is currently executing. The table also contains the amount of processing level that is required to execute each task. The processor determines whether it is busy or not based on the values in the task table [column 2, line 32 – column 3, line 45].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cai et al., US Patent no. 6,631,474, teaches a system with high power and low power processors.

JP 06110857 A teaches a system with a high speed and a low speed processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Paul Yanchus
November 19, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100